Anish Jindal

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Objective

Computer Engineering student with a strong interest in low-level hardware-software interaction and security. Proven experience in cost-optimization, reverse engineering systems, and managing complex project timelines.

Education

Georgia Institute of Technology | Atlanta, GA *June 2026 – Present*
Bachelor of Science in Computer Engineering, GPA 4.00 Expected Graduation, May 2029

Skills

Programming: Java, C, C++, C#, Go, Verilog, Rust (novice), Python
Hardware: Raspberry Pi, Arduino, logic analyzer
Software: Ghidra, Binary Ninja, Saleae Logic, Rider, KiCad, GitHub, Linux
Communication: Technical documentation
Languages: English (native), Hindi (native)

Experience

Tutor Jackets | Atlanta, GA *September 2026 – Present*
Math and English Tutor

- Teach ahead-of-curriculum Precalculus, and facilitate SAT test prep and review across subject areas.
- Facilitated a C → A letter grade improvement

Darena Solutions | Chesterfield, MO *June – August 2023*
Web UI Testing Intern

- Implemented a suite of 40+ end-to-end UI tests for a health IT application in Playwright
- Integrated tests into GitHub Actions CI infrastructure
- Presented work and established guidelines for future testing to ensure software robustness

Projects

Vex V5 Serial | Vexide *Jan 2026 – Aug 2026*
Firmware reverse engineering and protocol reimplementation project for a control system.

- Reverse-engineered the embedded firmware of multiple parts of the VEX V5 and EXP control systems
- Implemented USB serial protocol support for the Vex Robotics AI Vision Sensor

Budget V5 | Independent Project *August 2025 – December 2025*
Independent project to reverse engineer and reimplement the wire protocol used between elements of a control system.

- Reverse engineered the Vex Smartport protocol using a logic analyzer and static analysis of firmware in Ghidra
- Wrote Saleae analysis plugins to aid dynamic analysis
- Designed a PCB and developed firmware implementing a compatible platform for 1/10th the cost of the commercial offering.

Activities

Nanotechnology & Photonics Society | Project Lead *June 2026 – Nov 2026*

- Researched laser dicing methodologies for wafer singulation, coordinating with campus space stakeholders
- Working to characterize fiber laser dicing utilizing a stylus profiliometer
- Optimized the dicing cut map for a 20% increase in wafer utilization, saving costs.

Silicon Jackets | Design Verification Member *Oct 2026 – Present*

- Completed an onboarding assignment involving the design, verification, and physical layout of a minimal RISC-V inspired core.
- Completed further training in UVM
- Contributing to implementation of a VIP for the Axi4 protocol